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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,803	12/28/2001	Hiroaki Nakaoka	60188-116	4146

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EXAMINER

HU, SHOUXIANG

ART UNIT PAPER NUMBER

2811

DATE MAILED: 08/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

10/028,803

Applicant(s)

NAKAOKA ET AL. 

Examiner

Shouxiang Hu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 June 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-32 is/are pending in the application.
- 4a) Of the above claim(s) 24-32 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on Dec. 28, 01 (the formal one) is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/099,195.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) Z.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Claims 24-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

Claim Objections

2. Claims 16-23 are objected to because of the following informalities and/or defects:

In claim 16, the term of "a concentration of the semiconductor layer" should read as: --a concentration of said impurity ions in said semiconductor layer--.

In claim 19, the term of "a concentration of the semiconductor layer" recited in step (b) should read as: --a concentration of said ions of an element in said semiconductor--.

In claim 19, the term of "a concentration of the semiconductor layer" recited in step (c) should read as: --a concentration of said impurity ions of a first conductivity type in said semiconductor layer--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art ("AAPA") in view of JP'064 (JP 3-32064, 2-12-91; of record) and/or Nandakumar et al. ("Nandakumar"; US 5,917,219).

AAPA (Figs. 11-12e; also see page 1, line 20, through page 5, line 22) discloses a method for fabricating a semiconductor device (SOI MOSFET), comprising the steps of: (a) forming an element isolation film (704) on an SOI substrate including at least an insulator layer (702) and a semiconductor layer (703); (c) forming a gate insulator film (705); (d) forming a gate electrode (707); and (e) forming source/region regions (709 and 710) of a second conductivity type.

AAPA does not disclose that the method can further comprise a step of forming a lattice defect region and a high concentration channel region with impurity ions of Indium. However, JP'064 teaches a method to form an n-channel SOI MOSFET (Fig. 1; also see its English abstract) with a first conductivity type (P-type) heavily doped channel region (33) at/near the interface between the semiconductor layer (3) and the insulator layer (2) for absorbing holes so as to improve the breakdown strength. In addition, the method of JP'064 naturally further comprises a step of diffusing and activating the p-type impurities (in region 33) and the n-type impurities (in regions 32

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and 31) through a heat treatment in order to enable the device to be functional normally.

And, one of ordinary skill in the art would readily recognize that a P-type impurity region can be readily and commonly formed with Indium ions for highly precise and stable doping profiles, as evidenced in the prior art such as Nandakumar (see col. 3, lines 28-34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a step of forming a heavily Indium-doped channel region into the method of AAPA, as taught in JP'064 and/or Nandakumar, so that an SOI MOSFET with improved breakdown strength and with desired precise and stable doping profile would be obtained. And, in such a collectively taught method, the Indium heavily doped region also naturally forms a lattice defect region.

Regarding claim 18, it is noted that a large single crystal can always be regarded as being formed of multiple small single crystals.

5. Claims 19-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art ("AAPA") in view of JP'064 (JP 3-32064, 2-12-91; of record) and/or Nandakumar et al. ("Nandakumar"; US 5,917,219), as applied to claims 16-18 above, and further in view of JP'886 (JP 10-12886; 1-16-98; of record).

The disclosures of AAPA, JP'064 and Nandakumar are discussed as applied to claims 16-18 above.

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Although AAPA, JP'064 and Nandakumar do not expressly teach to further comprise a step of implanting Si or Ar ions to form lattice defect regions at/near the interface between the semiconductor layer and the insulator layer, JP'866 teaches to a method comprising such an implantation step for forming recombination centers to suppress the adverse floating effect (see the lattice defect region 11; also see the English abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further incorporate the recombination-center forming step of JP'886 into the method collectively taught by AAPA, JP'064 and Nandakumar above, so that an SOI MOSFET with suppressed adverse floating effect would be obtained.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
August 10, 2003


SHOUXIANG HU
PRIMARY EXAMINER